

ISL97693IRTZ-EVALZ Evaluation Board User Guide

The ISL97693 is Intersil's highly integrated 6-channel LED driver for display backlighting. This part maximizes battery life by featuring only 1mA quiescent current, and by operating down to 2.4V input voltage, with no need for higher voltage supplies.

Quick Start Guide

Please follow the following instructions and reference Figures 2 and 3.

1. Before applying power to the evaluation board, connect a power supply to the board by connecting the (+) positive terminal of the power supply to "VIN" and the (-) negative terminal to "PGND". Optional: To measure IVIN, connect the ammeter to JP_IC VIN on the evaluation board.
2. The "EN" pin is connected to one end of a mechanical switch on the evaluation board called "SW_EN". The other end of the switch is connected to the pin of the ISL97693. There is no need to connect a GND/power supply voltage to the "EN" pin since "VIN" on the evaluation board is directly tied to EN when "SW_EN" is put in the "H" position for LED ON, and the "L" position for LED OFF.
3. To measure (sense) the voltage at "VIN" on the evaluation board, place a voltmeter between "VIN" and "PGND". Connect the (+) positive terminal of the voltmeter to "VIN" and the (-) negative terminal to "PGND".
4. Optional: To measure the output voltage of the LED driver, place a voltmeter between "VOUT" and "PGND" on the evaluation board. Connect the (+) positive terminal of the voltmeter "VOUT" and the (-) negative terminal to "PGND".
5. Optional: To measure the output current (to the LED strings), place an ammeter between the pins of jumper "JP_IOUT". Connect a wire clip from one of the pins associated with "JP_IOUT" to the ammeter and another wire clip from the ammeter to the other pin associated with "JP_IOUT".
6. For 100% brightness, place 3.3V or 5V on the "PWMI" pin by connecting the (+) positive terminal of the power supply to "PWMI" and the (-) negative terminal to "PGND" on the evaluation board. For dimming, a function or pulse generator can be used to generate a PWM signal. Set the function generator to the "square wave" option and use an oscilloscope to verify that the amplitude, duty cycle, and PWM waveform are set to the desired setting. The amplitude of the PWM waveform needs to be GND reference (0V) with an amplitude range of 3.3V to 5V. Once the PWM waveform is set, place the (+) positive terminal from the function/pulse generator to "PWMI" pin and the (-) negative terminal to "PGND".
7. A potentiometer "ISET_R" is used to set the output current of the LED driver. Adjusting "ISET_R" will either decrease or increase the output current of the LED driver. Too much output current will result in the LED driver hitting the current limit, which is set internally by the IC.

8. Once steps 1-7 have been applied to the evaluation board, turn on the power supply and adjust the input voltage (2.4V~5.5V) for the desired setting.

Boost Switching Frequency and OVP Setting

The Boost switching frequency and over voltage protecting (OVP) voltage settings are:

1. Boost Switching Frequency Adjustment: Currently, the ISL97693IRTZ-EVALZ board has a resistor R7= 124kΩ, which sets the boost switching frequency $f_{SW} = 700\text{kHz}$ with Equation 1.

$$f_{SW} = \frac{(8.65 \times 10^{-10})}{R_{FSW}} \quad (\text{EQ. 1})$$

- f_{SW} is the desirable boost switching frequency (Hz)
- R_{FSW} is resistor from FSW pin to GND (Ω)

2. OVP Threshold Setting: The OVP level can be set based on Equation 2. The boost can regulate down to 30% of OVP. The OVP level should be determined considering LED string max forward voltage, and low temperature margin.

$$\text{OVP} = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad (\text{EQ. 2})$$

Please refer to the [ISL97693](#) datasheet for detailed switching and regulation adjustment.

LED Current Setting and Analog Dimming

The max LED current is set by using a resistor to AGND on the "ISET" pin. This resistor RSET is calculated using Equation 3:

$$I_{LEDmax} = 1066 / RSET \quad (\text{EQ. 3})$$

where:

RSET (Ω): The resistance from the "ISET" pin to "GND"

ILEDmax (A): The peak current set by resistor RSET

For example, if the required max LED current (ILEDmax) is 20mA, then the RSET value needed is:

$$RSET = 1066 / 0.02 = 53.3\text{k}\Omega \quad (\text{EQ. 4})$$

Choose the nearest standard resistor: 53.3kΩ, 0.1%

Using the concept above, DC dimming (also called analog dimming) can be accomplished by applying a DC voltage VDIM to the "ISET" pin via a resistor (see Figure 1):

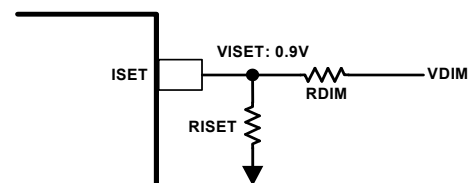


FIGURE 1. ANALOG DIMMING CONFIGURATION



FIGURE 2. PICTURE OF ISL97693IRTZ-EVALZ BOARD

If the VDIM is above VISET = 0.9V, the brightness will reduce, and vice versa.

NOTE: The LED driver calibrates itself at start-up, so it is important that the control voltage be set to the maximum brightness level when the ISL97693 is enabled, even if the LEDs are not ON at this point.

How to Setup the ISL97693 to Run 2-cell Battery In Series

1. It is important that “VIN” stay below the absolute rating of 5.5V.
2. Remove the jumper on “JP_IC_VIN” to the left of the inductor.
3. Using two power supplies, connect the power supply to the positive terminal to the right pin of JP_IC_VIN. Connect the negative terminal to “PGND” and the second power supply positive terminal to the “VIN” post. Connect the negative supply to “AGND”.
4. Remember that the IC can be damaged if “JP_IC_VIN” > 5.5V.
5. With this configuration, the second power supply that is connected to the “VIN” can go above 5.5V and is capable of running a 2S battery configuration.

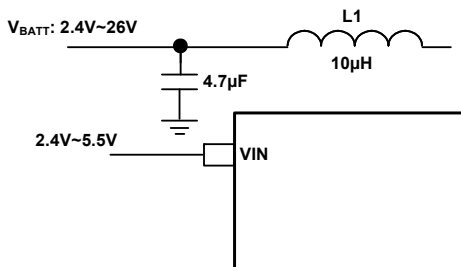


FIGURE 3. 2-CELL BATTERY SUPPLY CONFIGURATION

Small Sized Evaluation Board

The small sized ISL97693IRTZ-EVALZ board can be used to evaluate the device in an optimized application-like form factor. Refer to Figure 6.

PCB Layout with TQFN Package

Layout consideration is needed in designing a PC board for stable ISL97693 operation. As shown in the typical application diagram in Figure 5, the separation of PGND and AGND is essential, keeping the AGND, see Figure 5. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors from high current flow in resistive PCB traces. PGND and AGND should be on the top and bottom layers respectively in the two layers of the PCB. A star ground connection should be formed by connecting the LED ground return and AGND pins to the thermal pad with vias. The bottom plane then forms a quiet analog ground area that both shields components on the top plane, as well as providing easy access to all sensitive components. For example, the ground side of the FSW and ISET resistor can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be large to dissipate the required power. For multi-layer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

Figures 7 and 8 show examples of the evaluation board PCB layout. Figures 9 and 10 show small form factor PCB layout to be suitable for portable application. This type of layout is particularly important for this type of product, with high current flow in the main loop's traces. Here are additional layout considerations:

1. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input, and output connected with low impedance and wide metal is very important to keep these nodes closely coupled.
2. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close to the VIN pin.
3. For optimum load regulation and true VOUT sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the

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pin. The AGND connection of the lower OVP components is critical for good regulation.

4. The COMP network and all analog function components (on ISET, FSW, etc.) should be referenced to AGND.
5. The heat of the chip is mainly dissipated through the exposed thermal pad so maximizing the copper area around the thermal pad is a good idea. The thermal ground pad should be connected to system ground. A solid ground is helpful for the thermal and EMI performance.
6. The inductor, input and output capacitors should be mounted as tightly as possible to reduce the mechanical vibration. This reduces the audible noise and inductive ringing.

General Power PAD Design Considerations

Figure 4 shows an example of how to use vias to remove heat from the IC. We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad foot print with vias spaced such that the centre to centre spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

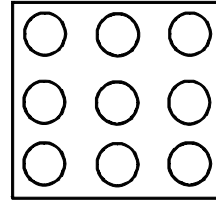


FIGURE 4. EXAMPLE OF POWER PAD

Schematics

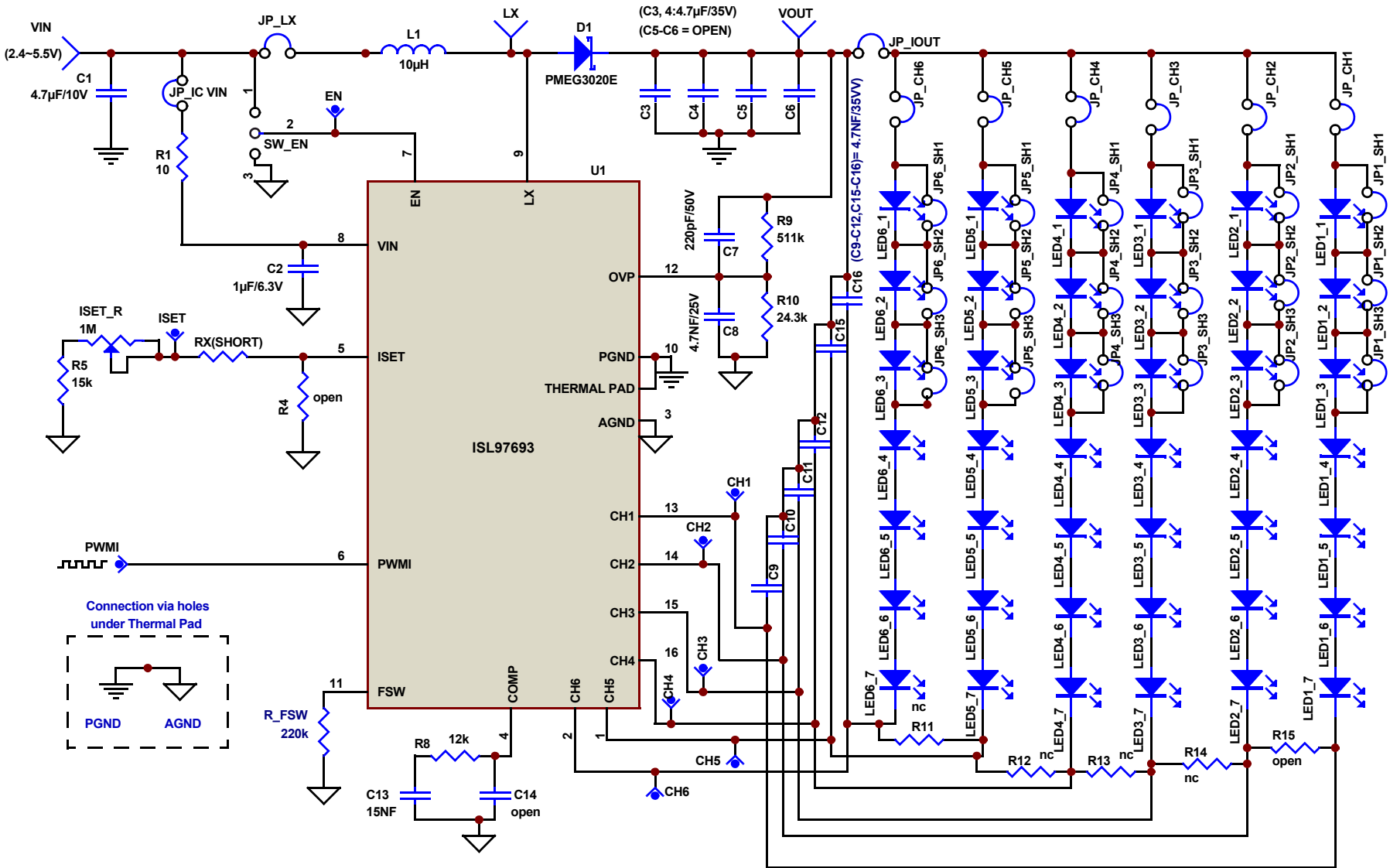


FIGURE 5. SCHEMATIC OF ISL97693IRTZ-EVALZ BOARD

Schematics (Continued)

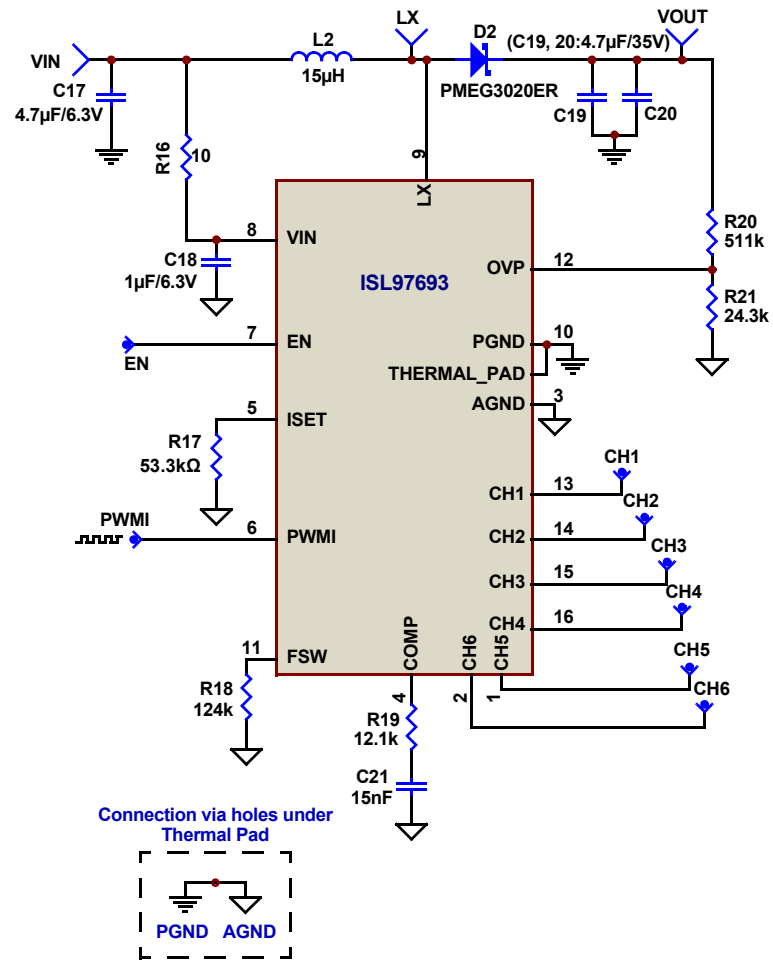


FIGURE 6. SCHEMATIC OF ISL97693IRTZ-EVALZ SMALL EVALUATION BOARD

Layout

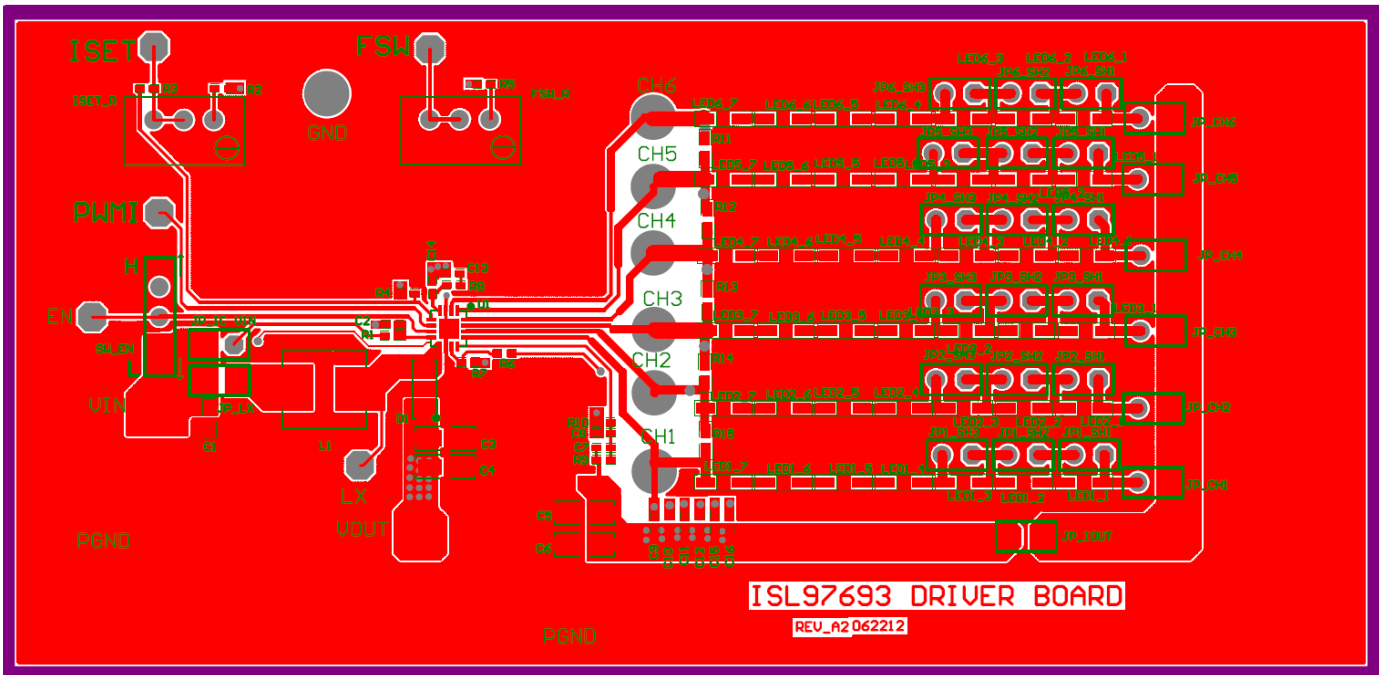


FIGURE 7. PCB LAYOUT (TOP LAYER) OF ISL97693IRTZ-EVALZ BOARD

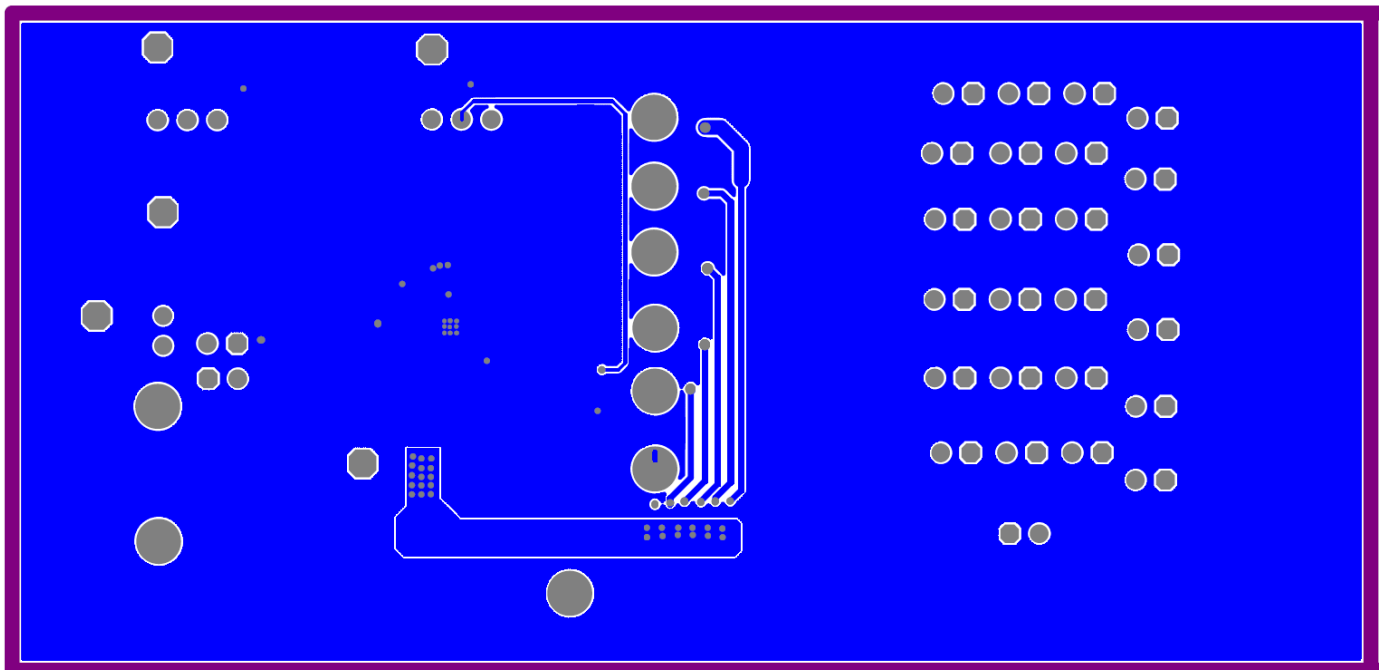


FIGURE 8. PCB LAYOUT (BOTTOM LAYER) OF ISL97693IRTZ-EVALZ BOARD

Layout (Continued)

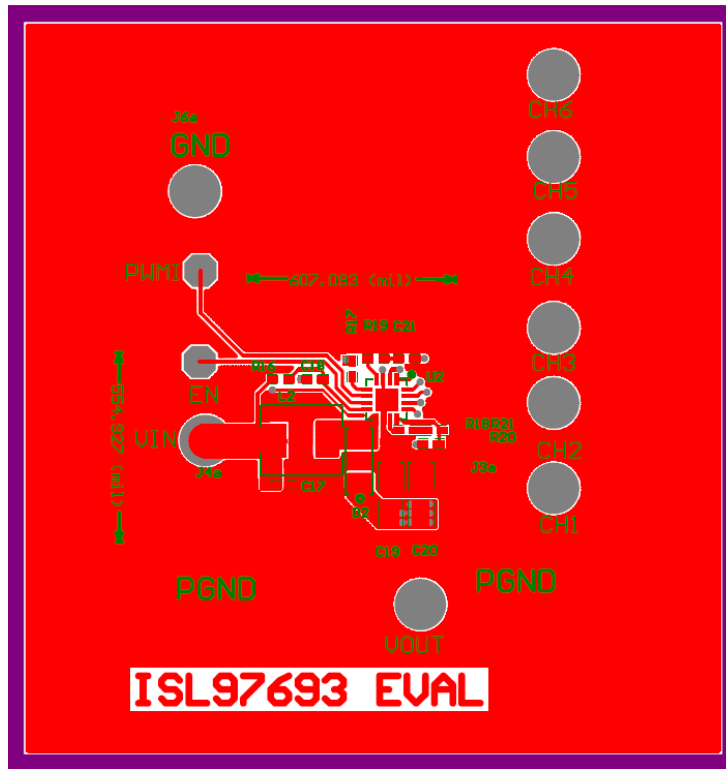


FIGURE 9. PCB LAYOUT (TOP LAYER) OF ISL97693IRTZ-EVALZ SMALL EVALUATION BOARD

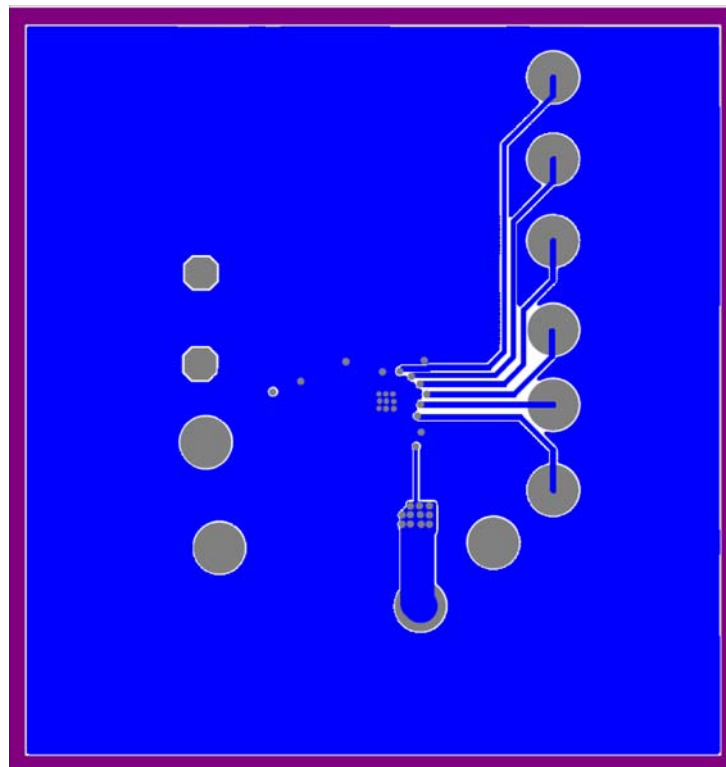


FIGURE 10. PCB LAYOUT (BOTTOM LAYER) OF ISL97693IRTZ-EVALZ SMALL EVALUATION BOARD

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TABLE 1. BILL OF MATERIALS FOR ISL97693 EVALUATION BOARD

PART TYPE	DESIGNATOR	FOOTPRINT
0Ω	R3	402
1M	ISET_R	VRES
1μF/6.3V	C2	402
4.7nF/25V	C8	402
4.7nF/50V	C9, C10, C11, C12, C15, C16	402
4.7μF/10V	C1	603
4.7μF/50V	C3, C4, C5, C6	805
10Ω	R1	402
12k	R8	402
15k	R2	402
15nF	C13	402
15μH	L1	PIMB061H-150MS
24.3k	R10	402
27k	R5	402
124k	R7	402
220pF/50V	C7	402
254k	FSW_R	VRES
511k	R9	402
ISL97693	U1	QFN16 3MM
LED-SMT	ALL LEDS	LW_Y87C
PMEG3020E	D1	SOD-123W

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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